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www.beyerlaw.com

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September 14, 2006

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Our Ref. No.:	10/693,223
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Appeal Brief – 23 Pages

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PAGE 1/26 * RCVD AT 9/14/2006 3:12:04 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-2/22 * DNIS:2738300 * CSID:5106630920 * DURATION (mm-ss):07-28

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Patton et al.

Application No.: 10/693,223

Filed: October 24, 2003

Title: SEQUENTIAL STATION TOOL FOR WET PROCESSING OF SEMICONDUCTOR WAFERS

Attorney Docket No.: NOVLP016C1/NVLS-2403C1

Examiner: Nguyen, Ha T.

Group: 2812

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APPEAL BRIEF TRANSMITTAL
(37 CFR 192)

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P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This brief is in furtherance of the Notice of Appeal filed in this case on July 14, 2006.

This application is on behalf of

☐ Small Entity ☒ Large Entity

Pursuant to 37 CFR 1.17(f), the fee for filing the Appeal Brief is:
☐ $250.00 (Small Entity) ☒ $500.00 (Large Entity)

☐ Applicant(s) hereby petition for a _____ extension(s) of time to under 37 CFR 1.136.

If an additional extension of time is required, please consider this a petition therefor.

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☒ Applicant(s) believe that no (additional) Extension of Time is required; however, if it is determined that such an extension is required, Applicant(s) hereby petition that such an extension be granted and authorize the Commissioner to charge the required fees for an Extension of Time under 37 CFR 1.136 to Deposit Account No. 500388.

Total Fee Due:

Appeal Brief fee	$500.00
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☐ Enclosed is Check No. in the amount of $.

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Respectfully submitted,
BEYER WEAVER & THOMAS, LLP

Jeffrey K. Weaver
Reg. No. 31,314

Anna Gavrilova
Reg. No. 58,181

P.O. Box 70250
Oakland, CA 94612-0250
(510) 663-1100

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

EX PARTE PATTON *et al.*

Application for Patent

Filed: October 24, 2003

Serial No. 10/693,223

FOR:

SEQUENTIAL STATION TOOL FOR WET PROCESSING OF SEMICONDUCTOR WAFERS

APPEAL BRIEF

CERTIFICATE OF FACSIMILE TRANSMISSION
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Signed: Cherryce R. Brown

Art unit: 2812
Examiner: Nguyen, Ha T.

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(1) REAL PARTY IN INTEREST

The real party in interest is NOVELLUS SYSTEMS, INC., the assignee of record.

Address: 4000 North First Street, San Jose, CA 95134

(2) RELATED APPEALS AND INTERFERENCES

N/A

(3) STATUS OF CLAIMS

There are a total of 13 claims pending in this application (claims 28-38 and 40-41). Claims 1-27 and 39 have been cancelled. Claims 28-38 and 40-41 were examined and rejected. No claims have been allowed.

Claims 28, 30-32, and 35-41 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over US Patent No. 6,344,129 issued February 5, 2002 to Rodbell et al. (hereinafter "Rodbell") in view of US Patent No. 6,017,820 issued January 25, 2000 to Ting et al. (hereinafter "Ting") and further in view of US Patent Application No. 09/812,229 published on January 10, 2002 (Publication No. 2002/0004265) by Vepa et al. (hereinafter "Vepa"). Claim 29 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Rodbell in view of Ting and Vepa, and further in view of US Patent No. 6,179,982 issued January 30, 2001 to Ting et al. (hereinafter "US982"). Claims 33-34 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Rodbell in view of Ting and Vepa, and further in view of US Patent No. 6,893,550 issued May 17, 2005 to Dubin et al. (hereinafter "Dubin")

There are no other rejections. The rejection of each of claims 28-38 and 40-41 under § 103 is appealed.

(4) STATUS OF AMENDMENTS

No amendment has been filed in response to the final rejection mailed on April 21, 2006.

(5) SUMMARY OF CLAIMED SUBJECT MATTER

The present invention is directed to methods of sequential wet processing of semiconductor wafers in a module or cluster tool. Specifically, it relates to integrated circuit fabrication methods that involve multiple electrochemical operations, including electroplating and an electrolytic material removal process such as electromechanical polishing. In some embodiments, these electrochemical operations as well as a wet etching operation are performed in a single module or cluster tool, albeit at different stations. The claimed invention focuses on two embodiments of these methods presented by independent claims 28 and 41.

Independent claim 28

Claim 28, one of the two independent claims on appeal, recites the following six operations:

(a) providing the wafer to an electrofill station in a module or cluster tool;

(b) in the electrofill station, electroplating copper on the wafer to fill high aspect ratio features;

(c) transferring the wafer to a second station in said module or cluster tool;

(d) in the second station, at least partially electromechanically polishing or electroplanarizing the wafer;

(e) transferring the wafer to another station in said module or cluster tool; and

(f) in the other station, wet etching the wafer.

Operation (a) of the claimed invention provides the wafer to an electrofill station in a module or cluster tool. This operation is described at page 15, line 25. A detailed description of an exemplary cluster tool having modules suitable for performing the claimed method is presented at page 20, lines 14-27. A single module of a cluster tool is described at page 9, line 4 to page 13, line 13. A cluster tool 401 is illustrated in Figure 4 and a single module 101 is illustrated in Figure 1. Typically, each module performs an encompassing process associated with integrated circuit fabrication, which in turn encompasses multiple sequential sub-processes. In one example, the entire module of a cluster tool is performing various sub-processes of electroplating operation (see page 10, lines 3-4). These subprocesses may include wetting, initiation, and electrofilling operations. Referring to an example shown in Figure 1, an electrofill station is illustrated by the component 115.

Operation (b) is performed in the electrofill station, and involves electroplating copper on the wafer to fill high aspect ratio features. This concept is described, for example, at page 15, lines 25 – 27, wherein electrofill is presented as one of the sub-processes of an encompassing electroplating process. In the example, illustrated by Figure 1, electroplating copper on the wafer to fill high aspect ratio features is performed in station 115.

Operation (c) involves transferring the wafer to a second station in the module or cluster tool. The wafer can be transferred either between stations within one module or between separate modules of one cluster tool. See page 9, line 32 to page 10, line 18 for an example of a wafer transfer mechanism within one module, and page 20, lines 14-27 for an example of a wafer transfer mechanism between modules within a cluster tool. In one implementation, the stations are located within a module in a carousel (radial) format. The wafer can be transferred from one station to the next by rotating the carousel with respect to the wafer holder/handler assembly, so as to situate the wafer above the selected station and then introduce the wafer to the selected station. In one example, the modules can also have a radial arrangement within the cluster tool, allowing a rotating robot arm to transfer wafers between the modules, e.g., as shown in Figure 4.

After the wafer has been transferred to the second station, operation (d) is performed in the second station. This operation involves at least partially electromechanically polishing or electroplanarizing the wafer. Electromechanical polishing and electroplanarization are among the processes that can be used during wet processing of the wafer. They can be advantageously integrated into the sequential wet processing method of the present invention and can be implemented using a wet processing module or cluster tool. These processes are referred to at page 21, lines 26-27.

Operation (e) involves transferring the wafer to another station in the module or cluster tool. This operation can be performed as described above (see for example page 9, line 32 to page 10, line 18, and page 20, lines 14-27).

Next, in an operation (f), the wafer is subjected to wet etching in the station it has been transferred to. Wet etching is a useful process that can complement electrochemical operations during integrated circuit fabrication. It is desirable to perform this process in conjunction with electrofill and electroplanarization processes in a sequential and high throughput manner that can be achieved by using a module or a cluster tool described in the present patent application. Wet etching is referred to, for example, at page 5, lines 25 - 30, and page 20, lines 2-7.

Dependent claims 29-38 and 40

Each of claims 29-38 and 40 depends directly or indirectly from claim 28.

Claim 29 specifies that "the electrofill station employs an electrofill electrolyte and the second station employs a second electrolyte, wherein the electrofill electrolyte and the second electrolyte have different compositions." As stated at page 10, lines 31-33, different stations may have separate plating baths. Having separate baths with distinct electrolyte compositions allows one to optimize the plating bath chemistries for particular subprocesses. Specifically, an electropolishing bath is referred to at page 20, lines 10-13.

Claims 30 and 31 recite that "copper is electroplated on the wafer to at least partially fill low aspect ratio features not completely filled during electroplating in the electrofill station"; and that this operation may be performed at a station other than the electrofill station. In an example described at page 18, lines 3-5, the low-aspect ratio features are filled in an overburden sub-process that is performed at a station, that is different from the "bottom-up" electrofill station. Referring to an example presented in Figure 1, high aspect ratio features are filled in an electrofill station 115 while low aspect ratio features are filled in an overburden station 117.

It is advantageous to use different electrolyte compositions for electroplating high and low aspect ratio features of the wafer. Claims 32 – 34 specify the electrolyte composition of the electrofill station.

Claim 32 recites that "the electrofill station includes an electrolyte comprising an additive." Support for this claim can be found at page 15, line 26-28.

Claim 33 specifies that "the additive comprises a suppressor, an accelerator, or both." This claim is supported in the specification at page 15, lines 27-28.

Claim 34 further specifies that "the accelerator is selected from the group consisting of MPS, SPS, and DPS." These compounds as well as their structural formulas are listed on page 16, lines 5-20.

It is desirable to use additives in the electrofill operation, since organic additives such as accelerators and suppressors are combined with copper salts in the electrolyte to slow copper deposition rate at the edges of the via and trench features. This effectively enhances the copper deposition rate at the bottom of those features and thus they fill with electrodeposited copper from the bottom up.

In contrast to high aspect ratio electrofill operation, electroplating on low-aspect ratio features typically does not require the use of additives.

Claim 35 states that in a method of claim 32, "the station in which copper is electroplated on the wafer to at least partially fill low aspect ratio features includes an electrolyte containing little or no additives." In this station the conditions are typically optimized for a higher deposition rate, and therefore use of additives is not recommended. For example, see page 18, lines 8 – 9 and lines 17-18.

As it was discussed above, wet processing of the wafer can be performed in a cluster tool having multiple modules dedicated to distinct processes.

Claim 36 specifies that "the method is performed in an apparatus comprising separate modules for electroplating and polishing or planarization." For example, separate modules for these processes are described at page 21, lines 4-5. Referring to Figure 4, the cluster tool 401 includes a plating module 409 and an electromechanical polishing or electroplanarization module 421.

Claim 37 recites that "the electromechanically polishing or electroplanarizating is performed sequentially using a plurality of stations." As it is described at page 6, lines 18-21, at least one of the modules of a cluster includes a sequential collection of station. These stations are used to sequentially perform sub-processes of an encompassing process. In this case, electroplanarization or electromechanical polishing is an encompassing process that can be sequentially performed using a plurality of stations in a module.

Claim 38 specifies that the method of processing a semiconductor wafer further comprises "performing metal chemical etching on the semiconductor wafer." For example, at page 20, lines 4-5, metal chemical etching is listed as one of the wet processing operations, that can be integrated into the sequential wet processing method performed in a module or a cluster tool.

In a similar vein, claim 40 specifies that the method of processing a semiconductor wafer further comprises "etching the semiconductor wafer to remove copper from the wafer's edge bevel and/or backside region." As it is described at page 20, lines 7-8, edge bevel removal operation and wafer backside etching are among the wet processes that can be advantageously incorporated into the sequential wet processing method of the present invention.

Independent claim 41

An independent claim 41 specifies a particular embodiment of a semiconductor wafer processing method. The method of claim 41 recites the following four operations:

(a) providing the wafer to an electrofill station where copper is electroplated on the wafer to fill high aspect ratio features;

(b) providing the wafer to a second plating station where copper is electroplated on the wafer to cover low aspect ratio features not filled during electroplating in the electrofill station;

(c) electromechanically polishing or electroplanarizing the wafer sequentially using a plurality of stations,

wherein (a) – (c) are performed in an apparatus comprising separate modules for electroplating and planarization; and

(d) wet etching the wafer in another station.

The independent claim 41 combines some concepts presented in claims 28, 31, 36 and 37 discussed above. Operation (a), for example, is presented similarly in claim 28 and is described in the specification at page 15, lines 25 - 27. Operation (b) is presented similarly in claim 31 and is illustrated in an "overburden" process at page 18, lines 3-5. Operation (c) generally corresponds to an operation presented in claim 37 and is supported in the specification at page 6, lines 18-21. As described at page 21, lines 4-5, and in claim 36 some of the operations of the claimed method can be performed in an apparatus comprising separate modules for electroplating and planarization. Finally, operation (d) generally corresponds to operation (f) of claim 28 and is supported in the specification at page 5, lines 25 - 30, and at page 20, lines 2-7.

(6) GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

There are three grounds of rejection to be reviewed on appeal:

Claims 28, 30-32, and 35-38 and 40-41 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Rodbell (US Patent No. 6,344,129) in view of Ting (US Patent No. 6,017,820) and further in view of Vepa (Publication No. 2002/0004265).

Claim 29 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Rodbell in view of Ting and Vepa, and further in view of US982.

Claims 33-34 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Rodbell in view of Ting and Vepa, and further in view of Dubin.

The rejected claims do not stand or fall together and each will be argued separately.

(7) ARGUMENT

Rejection of claims 28, 30-32, 35-38 and 40-41 under 35 U.S.C. § 103(a)

Introduction

Claims 28, 30-32, 35-38 and 40-41 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Rodbell in view of Ting and further in view of Vepa. Each appealed claim is separately patentable and the patentability of each will be argued separately. The Appellants' explanation of the differences between the above-cited references and the claimed invention will first be discussed for claim 28, and then for the dependent claims, each of which recites an additional limitation not found or suggested in the context of the cited references.

Claim 28

Claim 28, one of the two independent claims on appeal, recites the following six operations:

(a) providing the wafer to an electrofill station in a module or cluster tool;

(b) in the electrofill station, electroplating copper on the wafer to fill high aspect ratio features;

(c) transferring the wafer to a second station in said module or cluster tool;

(d) in the second station, at least partially electromechanically polishing or electroplanarizing the wafer;

(e) transferring the wafer to another station in said module or cluster tool; and

(f) in the other station, wet etching the wafer.

The primary reference (Rodbell) cited by the Examiner is directed to methods of forming copper plugs having a short resistance transient. These plugs are formed by electrofilling high-aspect ratio features of a semiconductor wafer with copper

under specific conditions. Rodbell does not disclose the use of modules or cluster tools in conjunction with his method, nor does it disclose material removal operations, such as electroplanarization, electromechanical polishing or wet etching. As stated by the Examiner in the last Office Action, Rodbell fails to disclose expressly the steps (c), (d), (e), and (f) of claim 28.

The Ting reference is concerned with an "interface that allows cluster tools to be completely isolated from one another when two different environments are utilized." (Column 3, lines 33-37). For example, the interface may be employed to connect one cluster tool operating under vacuum and a different cluster tool operating at atmospheric pressure. Ting mentions that one of the cluster tools may be responsible for plating operations, and may involve electroplating and electropolishing in a multiple station processing chamber. Ting, however, does not envision wet etching operation to be performed in conjunction with electrochemical processing of the wafer in one module or cluster tool.

The Examiner uses the Vepa reference for its disclosure of etching in a multi-station apparatus. It should be appreciated that while the Applicants' claimed invention as well as Ting and Rodbell references are directed to methods of forming integrated circuits (IC) on the semiconductor wafer, the Vepa reference describes a process that does not involve forming the elements of an IC (e.g., vias, trenches and interconnects).

Vepa describes a method of cleaning and planarizing the semiconductor wafer that may be used as a substrate for IC fabrication, but that would only be done much later, typically at a different facility. The Vepa method is performed after the wafers are cut from cylindrical boules of single crystal silicon (such as those formed by a Czochralski growth process), but before the wafer is packaged and shipped to an IC fabrication facility. Vepa describes grind polishing, cleaning, and etching the semiconductor material in a multi-station tool in order to obtain a flat wafer surface that will be suitable for IC fabrication. Obviously, after the wafer is cut from the single crystal silicon boule, it does not contain any material other than the single crystal silicon itself. It is the object of Vepa's method to planarize the surface of single crystal silicon, so as to remove the defects (such as waviness of the surface or grind marks) that were introduced during cutting and grind polishing of the wafers. The process disclosed by Vepa does not involve depositing or removing metals, and provides no context whatsoever for use of electrochemical methods.

The combination of Rodbell, Ting and Vepa references would not lead one of skill in the art to the claimed invention. To reach the claimed invention from these

references would require too many leaps. It would also require too many special choices such as which operations to use, how to apply them, and how to arrange them sequentially. Reaching the claimed invention from Rodbell, Ting and Vepa could only be accomplished by using the invention as a template and then picking and choosing select features from these references and cobbling them together in a wholly unexpected manner.

When presented with these three references, one skilled in the art, would not be able to perceive that it is advantageous to combine wet etching with electrochemical operations (e.g. electrofill and electroplanarization) in one module or cluster tool. Particularly, the Vepa reference would not lead one skilled in the art to use wet etching in conjunction with electrochemical processing of the wafer during IC fabrication. The planarization and etching of single crystal silicon wafers described by Vepa is too remote from the electroplating and electropolishing methods used in IC fabrication, to suggest such combination.

It is known that manufacturers of integrated circuits typically purchase their wafers from wafer providers and are not likely to consider wafer production methods (such as Vepa's) to apply to IC fabrication. Semiconductor wafers are commodities purchased and consumed by IC manufacturers. Even if the method of Vepa is considered by one skilled in IC fabrication, it would not provide any motivation for combining wet etching with methods of Ting and Rodbell, at least, because Vepa is not etching or processing any material beyond the semiconductor material itself. Since Vepa's method does not involve deposition or removal of metal, it is impossible to see how Vepa's method alone or in combination with Ting and Rodbell may motivate one skilled in the art to envision wet processing of copper-containing semiconductor substrate that will include electrofill, electroplanarization, and wet etching operations.

For at least these reasons, integrating wafer electrochemical processing and wet etching in a single module or cluster tool is not rendered obvious by the combination of Rodbell, Ting and Vepa. Reversal of the 103(a) rejection is therefore respectfully requested.

Claim 30

Claim 30 specifies that "copper is electroplated on the wafer to at least partially fill low aspect ratio features not completely filled during electroplating in the electrofill station." While Rodbell describes a two-step electroplating process used

primarily for filling high-aspect ratio features, it is conceivable that during this two-step process low aspect ratio features may also be partially filled. However, Rodbell does not provide any motivation to combine his method with electroplanarization, electropolishing or wet etching operations. In this regard, claim 30 provides additional details to formation of integrated circuit, and therefore makes the Vepa reference describing the wafer production method even less applicable. A *prima facie* case of obviousness has not been made. Reversal of the rejection is earnestly solicited.

Claim 31

Claim 31 specifies that in the method of claim 30 "copper is electroplated on the wafer to at least partially fill low aspect ratio features at a station other than the electrofill station." Rodbell describes a two-step electroplating process that may inherently fill high-aspect and low-aspect ratio features and use separate chambers or separate plating baths to perform those steps. However, as mentioned before, Rodbell does not provide motivation to one skilled in the art to combine electroplating with material removal operations (electropolishing, electroplanarization, or wet etching). Ting is silent with regard to electroplating wafer features with different aspect ratios. Most importantly, the Vepa reference would not even remotely suggest to one skilled in the art to use wet etching in one module or cluster tool in conjunction with electroplating copper in different aspect ratio features, since Vepa's substrate does not contain any features that would need to be filled with copper. A *prima facie* case of obviousness has not been made. Reversal of the rejection is requested.

Claim 32

Claim 32 specifies that in the method of claim 31 "the electrofill station includes an electrolyte comprising an additive." While Rodbell describes the use of additives during high aspect ratio electrofill process, Ting is mute with this respect, and Vepa does not disclose electrofill at all. The combined three references would not direct one skilled in the art to integrate wet etching with electrofill in one module or cluster tool, at least because Vepa's reference does not provide any context for electrofill or any IC forming process. The additional complexity and detail of the electrofill station recited in this claim makes combination with Vepa's wafer producing apparatus even less appropriate. A *prima facie* case of obviousness has not been made for claim 32. Reversal of the rejection is requested.

Claim 35

Claim 35 recites that in the method of claim 32 "the station in which copper is electroplated on the wafer to at least partially fill low aspect ratio features includes an electrolyte containing little or no additives." While Rodbell discloses electroplating a layer of copper using an electrolyte with little or no additives, Ting does not mention low or high aspect ratio features or any particular electrolyte compositions used for electroplating. The Vepa reference does not provide any suggestion whatsoever that any type of electroplating may be used in conjunction with the cleaning/grinding/etching method described therein. The additional electroplating details recited in this claim render a combination of Rodbell with Ting and particularly with Vepa even less appropriate (in comparison with claims 28 and 32 for example). The three references if combined, do not render obvious claim 35. Reversal of the rejection is requested.

Claim 36

Claim 36 specifies that the method of claim 28 "is performed in an apparatus comprising separate modules for electroplating and polishing or planarization." While Ting discloses that electroplating and electropolishing may be performed in a multiple station processing chamber, Ting fails to disclose that these operations can be integrated with wet etching in a module or cluster tool. The Vepa reference would not suggest to one skilled in the art that wet etching can be combined with electroplating or electrochemical material removal techniques. The Vepa's method does not provide any suggestion that an etching step performed during wafer production on a substrate lacking vias, trenches, metal lines, or any other features of integrated circuit, would correspond to wet etching performed during IC formation and that it could be advantageously integrated with electrochemical methods of claim 36. A separate *prima facie* case of obviousness has not been made. Reversal of the rejection is requested.

Claim 37

Claim 37 specifies that in the method of claim 28 "electromechanically polishing or electroplanarizng is performed sequentially using a plurality of stations." While Ting mentions that electroplating and electropolishing can be performed in a multiple station processing chamber, he is silent with respect to the number of stations that may be used to perform any of these operations. Ting also fails to disclose that electromechanical polishing or electroplanarizing may include sequentially performed subprocesses. As noted before, Rodbell and Ting are silent with respect to wet etching

operation. As with some of the other dependent claims, the additional complexity in electrochemical processing as recited in claim 37 makes it less likely that one skilled in the art would think to morph Vepa's wafer production technology to a form that could be combined with the IC fabrication steps recited in either Ting or Rodbell. Therefore the combined Rodbell, Ting and Vepa references fail to suggest that wet etching can be used in one module or cluster tool with electrochemical processing of the wafer. Particularly, the Vepa reference would not guide one skilled in the art to use wet etching together with electrochemical methods of IC fabrication, since Vepa's reference provides only for an etching operation during wafer production and not during IC formation. Since electroplanarizing is not used or needed during wafer production, no suggestion to use wet etching in one cluster tool with electroplanarizing is provided. A separate *prima facie* case of obviousness has not been made. Reversal of the rejection is requested.

Claim 38

Claim 38 specifies that the method of claim 28 further includes an operation of "performing metal chemical etching on the semiconductor wafer." Contrary to the Examiner's comments provided in the last Office Action, Ting fails to disclose performing metal chemical etching on the semiconductor wafer. Neither Rodbell nor Vepa make reference to this operation. Therefore, the limitation of claim 38 is not disclosed or suggested by the combined Rodbell, Ting, and Vepa references. For at least this reason, claim 38 is separately patentable. Further, regardless of whether other references describing metal chemical etching exist, claim 38 provides additional details on the formation of integrated circuit features. The Vepa reference does not address metal etching or deposition, and would not motivate one skilled in the art to integrate wet etching, metal chemical etching and electrochemical methods of IC fabrication in one module or cluster tool. A separate *prima facie* case of obviousness has not been made. Reversal of the rejection is requested.

Claim 40

Claim 40 specifies that the method of claim 28 further includes an operation of "etching the semiconductor wafer to remove copper from the wafer's edge bevel and/or backside region." The Examiner makes reference to the Rodbell reference, while arguing the patentability of claim 40. Contrary to the Examiner's argument, neither Rodbell nor Ting nor Vepa, either alone or combined, disclose or suggest the limitation of etching the semiconductor wafer to remove copper from the wafer's edge bevel and/or backside region. For at least this reason, claim 40 is separately patentable. Further, regardless if other references describing edge bevel and/or

backside region removal exist, claim 40 provides additional details on the formation of integrated circuit features. The Vepa reference does not address formation of integrated circuit features at all, and would not motivate one skilled in the art to integrate wet etching, edge bevel and/or backside region removal and electrochemical methods of IC fabrication in one module or cluster tool. A separate *prima facie* case of obviousness has not been made. Reversal of the rejection is requested.

Claim 41

An independent claim 41 recites the following four operations:

(a) providing the wafer to an electrofill station where copper is electroplated on the wafer to fill high aspect ratio features;

(b) providing the wafer to a second plating station where copper is electroplated on the wafer to cover low aspect ratio features not filled during electroplating in the electrofill station;

(c) electromechanically polishing or electroplanarizing the wafer sequentially using a plurality of stations,

wherein (a) – (c) are performed in an apparatus comprising separate modules for electroplating and planarization; and

(d) wet etching the wafer in another station.

While Rodbell describes electrofill without making reference to the cluster tool or material removal methods, Ting mentions electroplating and electropolishing in a cluster tool without making reference to wet etching, and Vepa is concerned with grinding, etching and cleaning the wafer prior to formation of integrated circuit features, these three references would not lead one skilled in the art to conceive a method of claim 41. Only in hindsight, the method of claim 41 may seem to be suggested by these references. Without this hindsight, these three references would present an array of unrelated features. It is not obvious which of the multiple features presented in these references should be picked, why they should be selected, and how they should be used in a method that would have advantageous characteristics.

Particularly, one skilled in the art would not know what operations should be selected from the Vepa reference, why these operations should be used in a process that deals with formation of integrated circuit features, and how these operations

would fit into this process. The combined three references cited by the Examiner in the rejection of claim 41 do not suggest that electrochemical processing of the wafer and wet etching should be integrated in one cluster tool. A *prima facie* case of obviousness has not been made. Reversal of the rejection is earnestly solicited.

Rejection of claim 29 under 35 U.S.C. § 103(a)

In the rejection of claim 29 the Examiner uses a combination of Rodbell, Ting, and Vepa references as applied above. Further, the US982 reference is used as a secondary reference.

The US982 reference is directed to a processing chamber for electroplating and electropolishing material to/and from a semiconductor wafer. The US982 reference does not disclose a multi-station apparatus or a cluster tool. It does not overcome the problems, as explained above, in relying on the Rodbell, Ting, and Vepa references to reject claim 28.

Claim 29

Claim 29 specifies that in the method of claim 28 "the electrofill station employs an electrofill electrolyte and the second station employs a second electrolyte, and the electrofill electrolyte and the second electrolyte have different compositions." While the US982 reference mentions that different electrolytes may be used in the electroplating and electropolishing operations, it does not disclose a multi-station module or cluster tool. Most importantly, the combination of the Rodbell, Ting, Vepa and US982 references does not render claim 29 obvious, at least, for the reason that the combined teachings of these references, do not suggest using wet etching in conjunction with electrofill and electromechanical polishing. The additional details on electrolyte composition provided in claim 29 render the Vepa reference even less applicable, since Vepa reference is not directed to IC formation and does not provide any context for use of electroplating and electropolishing. A separate *prima facie* case of obviousness has not been made. Reversal of the rejection is requested.

Rejection of claims 33-34 under 35 U.S.C. § 103(a)

In the rejection of claims 33 and 34 the Examiner uses a combination of Rodbell, Ting, and Vepa references as applied above. Further, the Dubin reference is used as a secondary reference.

The Dubin reference is directed to copper electroplating bath compositions. It makes no reference to material removal methods or to the use of multi-station tools.

Claim 33

Claim 33 specifies that in the method of claim 32 "the additive comprises a suppressor, an accelerator, or both." While the Dubin reference describes the use of additives, it fails to provide any suggestion that combining a wet etching process with electrochemical wafer processing in one module or cluster tool would be advantageous. The additional IC processing features recited in claim 33 render it less likely that one skilled in the art would consider the Vepa reference together with the other references, which are directed to forming of IC features. As explained, even if all references were to be considered together, Vepa does not provide even a remote motivation to integrate wet etching with electrofill operation, wherein electrofill station has electrolyte that includes suppressors or accelerators. A separate *prima facie* case of obviousness has not been made. Reversal of the rejection is requested.

Claim 34

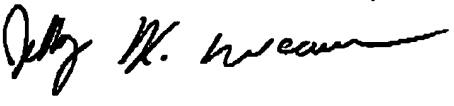
Claim 34 specifies that in the method of claim 34 "the accelerator is selected from the group consisting of MPS, SPS, and DPS." While the Dubin reference describes the use of these compounds during plating, it does not suggest that a wet etching process should be performed in one module or cluster tool with electroplating or electropolishing. Most importantly, the use of specific compounds during plating further defines the IC formation method and makes the Vepa reference even less likely to be considered by one skilled in the art, since Vepa's methods are outside of scope of IC forming methods. Therefore the combination of Rodbell, Ting, Vepa and Dubin does not render obvious claim 34, particularly the integration of wet etching and electrofill operations in one module or cluster tool. A separate *prima facie* case of obviousness has not been made. Reversal of the rejection is requested.

Conclusion

Appellants have pointed out that the cited references contain insufficient teachings to render the claims *prima facie* obvious. In combination, the references fail to suggest a method of processing a semiconductor wafer as claimed, without using the claims as a blueprint and recasting one or both of the reference's to something wholly unrelated to its original form. In order for the cited references to render the claims obvious, at least one of the references would have had to teach one of skill to integrate wet etching and electrochemical wafer processing operations in one module or cluster tool.

In view of the foregoing, it is respectfully submitted that none of the pending claims are rendered unpatentable by the Rodbell, Ting, Vepa, US982 and Dubin references. Accordingly, the pending rejections of all of the claims under 35 U.S.C. § 103 should be reversed.

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP



Jeffrey K. Weaver
Reg. No. 31,314

Anna Gavrilova
Reg. No. 58,181

P.O. Box 70250
Oakland, CA 94607-0250
(510) 663-1100

(8) CLAIMS APPENDIX

APPENDIX
PENDING CLAIMS

1-27. (Canceled)

28. (Previously presented) A method of processing a semiconductor wafer comprising:

(a) providing the wafer to an electrofill station in a module or cluster tool;

(b) in the electrofill station, electroplating copper on the wafer to fill high aspect ratio features;

(c) transferring the wafer to a second station in said module or cluster tool;

(d) in the second station, at least partially electromechanically polishing or electroplanarizing the wafer;

(e) transferring the wafer to another station in said module or cluster tool; and

(f) in the other station, wet etching the wafer.

29. (Previously presented) The method of claim 28, wherein the electrofill station employs an electrofill electrolyte and the second station employs a second electrolyte, and wherein the electrofill electrolyte and the second electrolyte have different compositions.

30. (Previously presented) The method of claim 28, wherein copper is electroplated on the wafer to at least partially fill low aspect ratio features not completely filled during electroplating in the electrofill station.

31. (Previously presented) The method of claim 30, wherein the copper is electroplated on the wafer to at least partially fill low aspect ratio features at a station other than the electrofill station.

32. (Previously presented) The method of claim 31, wherein the electrofill station includes an electrolyte comprising an additive.

33. (Previously presented) The method of claim 32, wherein the additive comprises a suppressor, an accelerator, or both.

34. (Previously presented) The method of claim 33, wherein the accelerator is selected from the group consisting of MPS, SPS, and DPS.

35. (Previously presented) The method of claim 32, wherein the station in which copper is electroplated on the wafer to at least partially fill low aspect ratio features includes an electrolyte containing little or no additives.

36. (Previously presented) The method of claim 28, wherein the method is performed in an apparatus comprising separate modules for electroplating and polishing or planarization.

37 (Previously presented) The method of claim 28, wherein the electromechanically polishing or electroplanarizating is performed sequentially using a plurality of stations

38. (Previously presented) The method of claim 28, further comprising performing metal chemical etching on the semiconductor wafer.

39. (Cancelled)

40. (Previously presented) The method of claim 28, further comprising etching the semiconductor wafer to remove copper from the wafer's edge bevel and/or backside region.

41. (Previously presented) A method of processing a semiconductor wafer comprising:

(a) providing the wafer to an electrofill station where copper is electroplated on the wafer to fill high aspect ratio features;

(b) providing the wafer to a second plating station where copper is electroplated on the wafer to cover low aspect ratio features not filled during electroplating in the electrofill station;

(c) electromechanically polishing or electroplanarizing the wafer sequentially using a plurality of stations,

wherein (a) – (c) are performed in an apparatus comprising separate modules for electroplating and planarization; and

(d) wet etching the wafer in another station.

(9) EVIDENCE APPENDIX

None.

(10) RELATED PROCEEDINGS APPENDIX

None.